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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,499	CALAFUT ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed April 25, 2006 has been entered. Claim 1 has been amended. Claims 12 and 13 have been added. Claim 11 has been withdrawn. Claims 1-13 are pending.

Drawings

2. The drawings were received on April 25, 2006. These drawings are acceptable.

Specification

3. Amendments have been made to the specification. Since the corrections are for typographical and inadvertent errors, the amendment to the specification is acceptable.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-10 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 17, recites: wherein the Schottky structure consumes **less than 5.0%** of the active area".

The phrase "less than" is indefinite because "less than" has no lower limit and caused the claim to read literally on embodiment outside the "2.5% to 5.0 %" range. See *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sapp (U.S. Patent No. 6,351,018) in view of Korman et al. (U.S. Patent No. 5,111,253) both of record.

With respect to claim 1, Sapp teaches a monolithically integrated structure combining a field effect transistor and a Schottky structure (210) in an active area of a semiconductor substrate substantially as claimed, wherein:

the field effect transistor comprises:

a first trench (200) extending into the substrate (202) and including a conductive material (206) forming a gate electrode of the field effect transistor; and

a pair of doped source regions (212) positioned adjacent to and on opposite sides of the trench (200) and inside a doped body region (214), the doped source regions (212) forming a source electrode of the field effect transistor, and the substrate (202) forming a drain electrode of the field effect transistor, and

the Schottky structure (210) comprises:

a pair of adjacent trenches (220-3; 200-4) extending into the substrate (202), the pair of adjacent trenches (200-3; 200-4) including a conductive material (206) which is separated from trench side-walls by a thin layer of dielectric (204); and

a Schottky diode having a barrier layer (218) formed on the surface of the substrate (202) and between the pair of adjacent trenches (200);

wherein the Schottky structure consumes a minimal portion of the active area, and the field effect transistor consumes the remaining portion of the active area. (See Figs. 2-7).

Thus, Sapp is shown to teach all the features of the claim with the exception of explicitly disclosing a specific percentage of area occupied by the Schottky structure.

Note that the specification contains no disclosure of either the *critical nature of the claimed Schottky structure consumes less than* $5.0^{\%}$ of active area of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Sapp also teaches: [S]ince the area of the Schottky diode determines it forward voltage drop in response to current, Schottky structures with different numbers of adjacent trenches can be devised to arrive at the desired area. (See col. 5, lines 3-6).

However, Korman teaches Schottky diode occupies between 5% and 50% of the active area. (See col. 8, lines 23-25). Note that, 5% also includes less than 5%, since the term is approximate.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the monolithically integrated structure of Sapp having an optimized active area consumes by the Schottky structure as taught by Korman to enhance the performance characteristic of the MOSFET switch, since such a modification would have involved a mere change in the size of a component, e.g., area consumes by the Schottky structure. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose,* 105 USPQ 237 (CCPA 1955).

Furthermore, within purview of one having ordinary skill in the art and as taught by Sapp, it would have been obvious to determine the optimum area consumes by the Schottky structure. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover **optimum or workable ranges** by routine experimentation.

With respect to claim 2, the field effect transistor of Sapp further comprises a metal layer (216) contacting the pair of doped source regions (212), the metal layer (216) and the barrier layer (218) comprise one of either titanium tungsten or titanium nitride.

With respect to claim 3, the barrier layer (218) and the metal layer (216) of Sapp contacting the source regions (212) connect together by an overlying layer of metal. (See Fig. 2).

With respect to claim 4, the barrier layer (218) of Sapp forms the Schottky diode anode terminal and the substrate (202) forms the Schottky diode cathode terminal.

With respect to claim 5, the integrated structure of Sapp further comprises a second trench (200) adjacent to the first trench (200), the second trench forming the gate electrode of the

field effect transistor in a similar fashion to the first trench, wherein a distance between the first trench (200) and the second trench (200) is greater than a distance W separating the pair of adjacent trenches (200-3; 200-4), and wherein the barrier layer (218) and a metal layer (216) contacting the source regions of the field effect transistor comprise one of either titanium tungsten or titanium nitride.

With respect to claim 6, the conductive material in the first and second trenches of Sapp electrically connects to the conductive material in the pair of adjacent trenches the Schottky diode is formed.

With respect to claim 7, the conductive material of Sapp in the pair of adjacent trenches between which the Schottky diode is formed is electrically isolated from the conductive material in the first and second trenches.

With respect to claim 8, the conductive material (206) of Sapp in the pair of adjacent trenches between which the Schottky diode is formed, is recessed into the pair of adjacent trenches and covered by a layer of dielectric material. (See Fig. 4).

With respect to claim 12, since 5% of Korman is seen as approximate 5% or less than 5.0%, thus, the limitation the claim is met. Further, the reason as discussed in claim 1 above also applies.

6. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sapp '018 and Korman '253 as applied to claim 1 above, and further in view of Hurst et al. (U.S. Patent No. 6,437,386).

Sapp teaches a monolithically integrated structure as described in claim 1 above including a first trench extending into the substrate, wherein an insulating layer (204) formed lining the side and bottom of the first trench.

Thus, Sapp is shown to teach all the features of the claim with the exception of the thickness of the insulating layer of the first trench as well as the pair of adjacent trenches along the bottom is thicker than that along the sidewalls.

However, Hurst teaches dielectric layer formed along the bottom (27) of a trench is thicker than that formed along the sidewalls (21) substantially reduces gate charge to reduce gate-to-drain capacitance thereby increasing the efficiency and prolong the life of the semiconductor device.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the insulating layer lining the trenches of Sapp thicker on the bottom than on the sidewalls as taught by Hurst to reduce gate-to-drain capacitance thereby increasing the efficiency and prolong the life of the semiconductor device.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sapp '018 and Korman '253 as applied to claim 1 above, and further in view of Baliga (U.S. Patent No. 5,998,833) of record.

Sapp teaches a monolithically integrated structure as described in claim 1 above including the first trench and the pair of adjacent trenches comprising conductive material.

Thus, Sapp is shown to teach all the features of the claim with the exception of explicitly one or more conductive electrodes beneath the conductive material.

However, Baliga teaches alternatively, the trenches can be made including at least one conductive electrode (26) formed under the conductive material (30). (See Fig. 4I).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the monolithically integrated structure of Sapp including one or more conductive electrode as taught by Baliga to reduce the gate-to-drain capacitance and improve switching speed.

Response to Arguments

8. Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER